

INN150FQ070A

1. General description

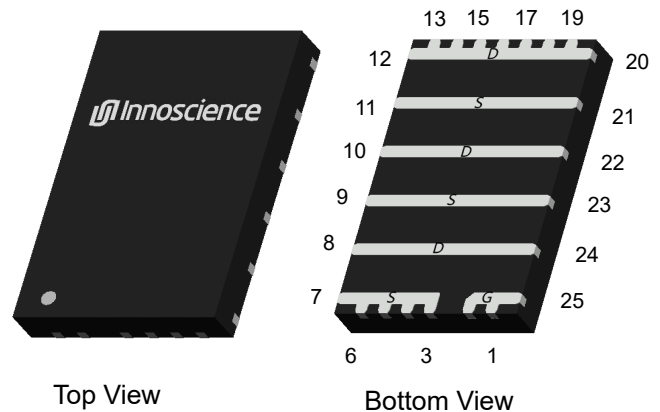
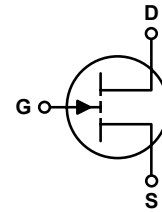
GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in FCQFN with 4.0 mm x 6.0 mm package size.

2. Features

- GaN-on-Silicon E-mode HEMT technology
- Industry Application
- Very low gate charge
- Ultra-low on resistance
- Very small footprint

3. Applications

- High frequency DC-DC converter
- Solar Systems optimizers and microinverters
- PD Charger and PSU Synchronous Rectification
- Telecom Power Supply
- Motor driver



4. Key performance parameters

Table 1 Key performance parameters at $T_J = 25\text{ }^{\circ}\text{C}$

Parameter	Value	Unit
$V_{DS,max}$	150	V
$R_{DS(on),max}$ @ $V_{GS} = 5\text{ V}$	7	m Ω
$Q_{G,typ}$ @ $V_{DS} = 75\text{ V}$	13	nC
$I_{DS,Pulse}$	160	A
Q_{OSS} @ $V_{DS} = 75\text{ V}$	75	nC

5. Pin information

Table 2 Pin information

Pin	Pin description	Pin function
1,2,25	Gate	Driver Gate
3-7,9,11,21,23	Source	Source
8,10,12-20,22,24	Drain	Power Drain

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN150FQ070A	FCQFN 4X6	M03

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6. Maximum ratings

at $T_J = 25^\circ\text{C}$ unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	150	V
$V_{DS(tr)}$	Drain-to-Source Voltage (up to 300,000 5ms pulse at 150°C)	180	V
I_D	Continuous current	60	A
	Pulsed (25°C , $T_{Pulse} = 100\ \mu\text{s}$)	160	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	$^\circ\text{C}$

7. Thermal characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
R _{θJC}	Thermal Resistance, Junction to Case	17.04	°C/W	-
R _{θJB}	Thermal Resistance, Junction to Board	2.42	°C/W	-
R _{θJA}	Thermal Resistance, Junction to Ambient ¹	53.04	°C/W	-
T _{sold}	Maximum reflow soldering temperature	260	°C	MSL3

Note 1: R_{θJA} is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

8. Electric characteristics

at $T_J = 25\text{ }^{\circ}\text{C}$, unless specified otherwise

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Voltage	150	-	-	V	$V_{GS} = 0\text{ V}$, $I_D = 1.4\text{ mA}$
I_{DSS}	Drain Source Leakage	-	1.5	150	μA	$V_{GS} = 0\text{ V}$, $V_{DS} = 150\text{ V}$
I_{GSS}	Gate-to-Source Forward Leakage	-	1.5	100	μA	$V_{GS} = 5\text{ V}$
	Gate-to-Source Forward Leakage	-	4.0	1000	μA	$V_{GS} = 6\text{ V}$
	Gate-to-Source Reverse Leakage	-	0.1	100	μA	$V_{GS} = -4\text{ V}$
$V_{GS(TH)}$	Gate Threshold Voltage	0.8	1.1	2.1	V	$V_{DS} = V_{GS}$, $I_D = 7\text{ mA}$
$R_{DS(on)}$	Drain-Source On-state Resistance	-	5.4	7	$\text{m}\Omega$	$V_{GS} = 5\text{ V}$, $I_D = 20\text{ A}$
V_{SD}	Source-Drain Forward Voltage	-	1.5	-	V	$I_S = 0.5\text{ A}$, $V_{GS} = 0\text{ V}$

Table 7 Dynamic characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{ISS}	Input Capacitance	-	1450	-	pF	$V_{GS} = 0\text{ V}, V_{DS} = 75\text{ V}$
C_{OSS}	Output Capacitance	-	525	-		$V_{GS} = 0\text{ V}, V_{DS} = 75\text{ V}$
C_{RSS}	Reverse Transfer Capacitance	-	7	-		$V_{GS} = 0\text{ V}, V_{DS} = 75\text{ V}$
$C_{OSS(ER)}$	Energy Related C_{OSS}	-	740	-		$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 75\text{ V}$
$C_{OSS(TR)}$	Time Related C_{OSS}	-	1000	-		$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 75\text{ V}$
R_G	Gate resistance	-	2	-	Ω	$f = 5\text{ MHz}$, open drain
Q_G	Total Gate Charge	-	13	-	nC	$V_{GS} = 5\text{ V}, V_{DS} = 75\text{ V}, I_D = 20\text{ A}$
Q_{GS}	Gate to Source Charge	-	3	-		$V_{DS} = 75\text{ V}, I_D = 20\text{ A}$
Q_{GD}	Gate to Drain Charge	-	2	-		$V_{DS} = 75\text{ V}, I_D = 20\text{ A}$
$Q_{G(TH)}$	Gate Charge at Threshold	-	1.5	-		$V_{DS} = 75\text{ V}, I_D = 20\text{ A}$
Q_{OSS}	Output Charge	-	75	-		$V_{GS} = 0\text{ V}, V_{DS} = 75\text{ V}$

9. Electric characteristics diagrams

at $T_J = 25\text{ }^{\circ}\text{C}$, unless specified otherwise

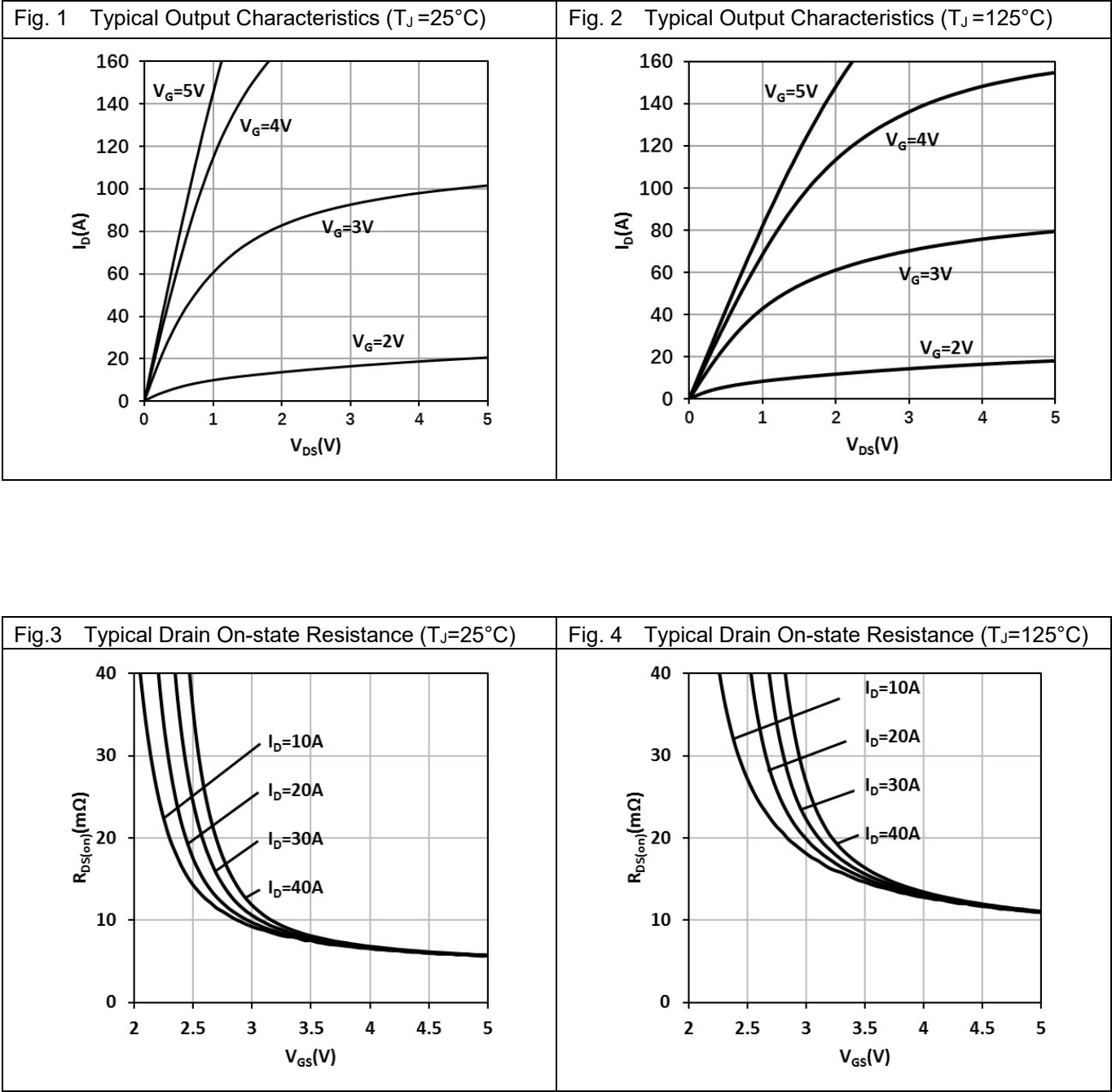


Fig. 5 Normalized On-State Resistance vs. Temp.

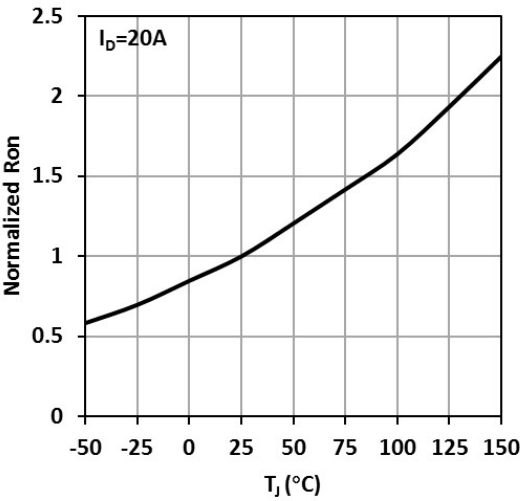


Fig. 6 Typical Transfer Characteristics

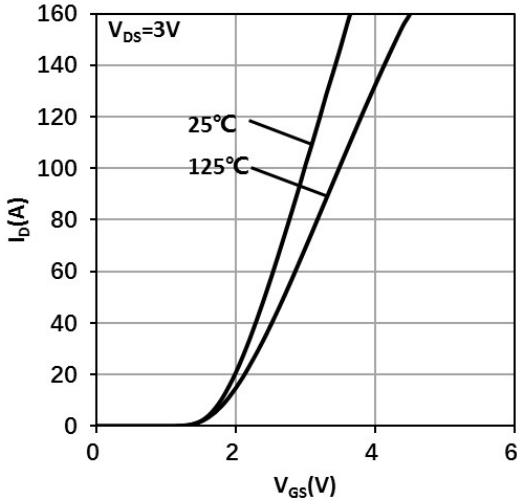


Fig. 7 Typ. Reverse Drain-Source Characteristics ($V_{GS} \leq 0$, $T_J = 25^{\circ}C$)

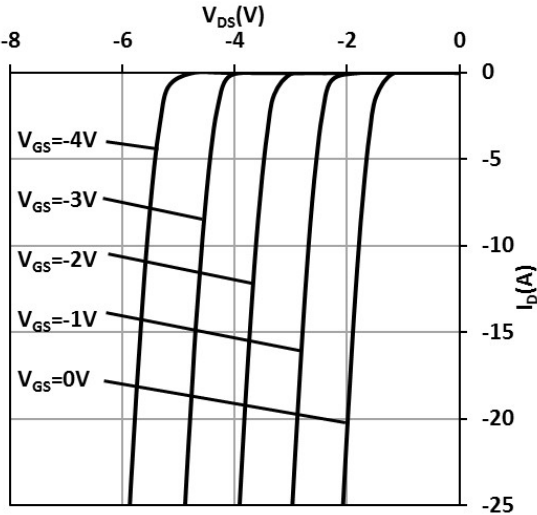


Fig. 8 Typ. Reverse Drain-Source Characteristics ($V_{GS} \geq 0$, $T_J = 25^{\circ}C$)

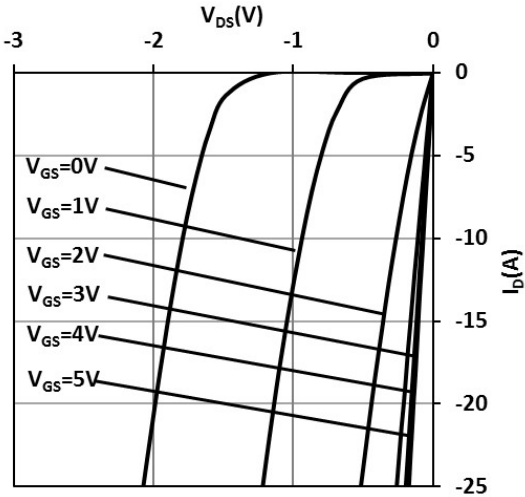


Fig. 9 Typ. Reverse Drain-Source Characteristics ($V_{GS} \leq 0$, $T_J = 125^\circ\text{C}$)

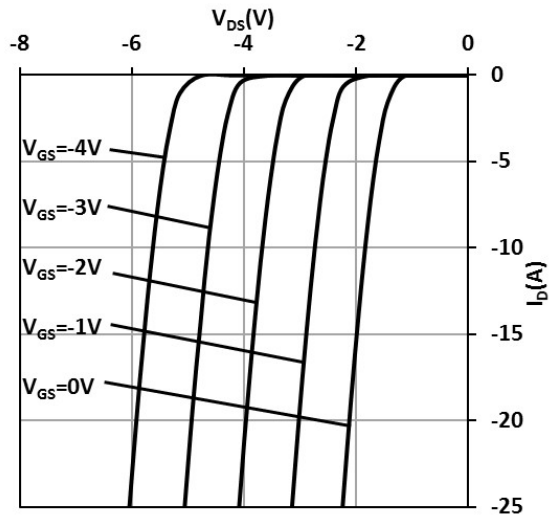


Fig. 10 Typ. Reverse Drain-Source Characteristics ($V_{GS} \geq 0$, $T_J = 125^\circ\text{C}$)

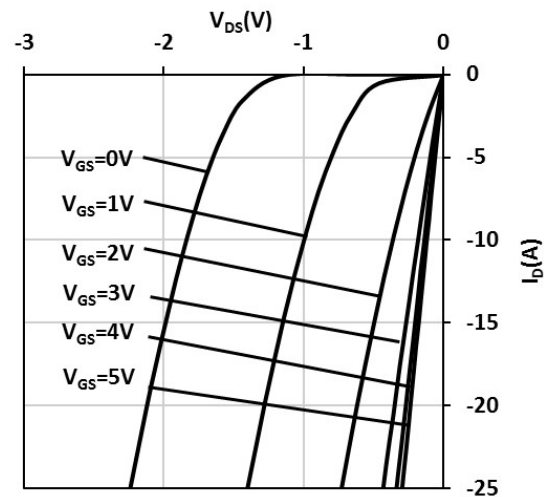


Fig. 11 Typ. Capacitances Characteristics

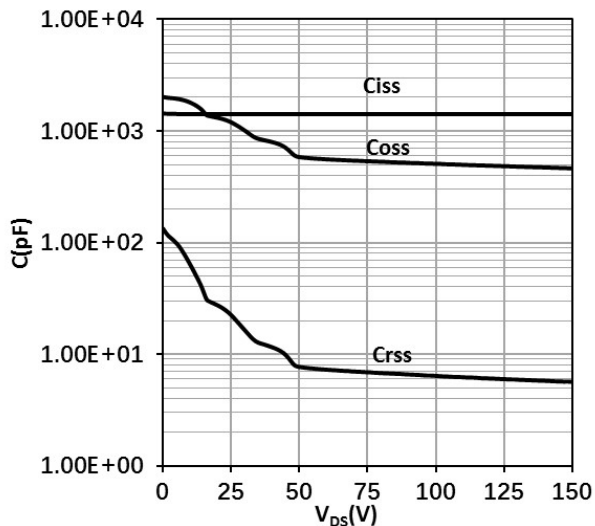


Fig. 12 Typ. Gate Charge

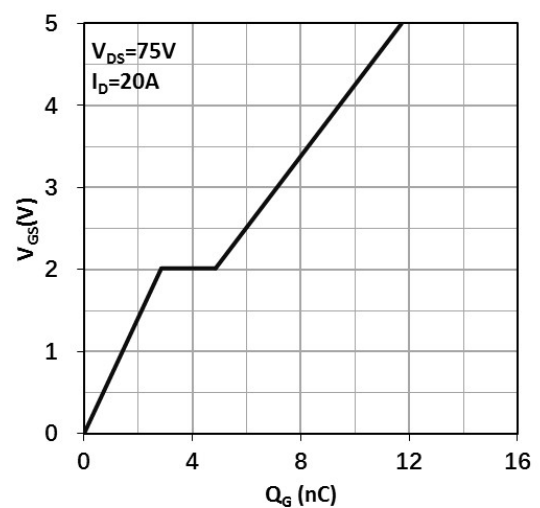


Fig. 13 Normalized Threshold Voltage vs. Temp.

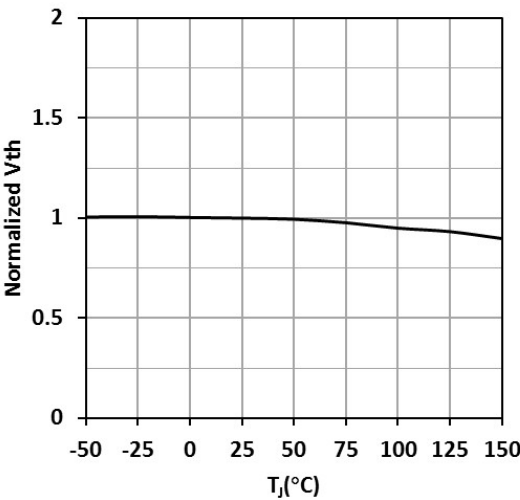


Fig. 14 Output Charge

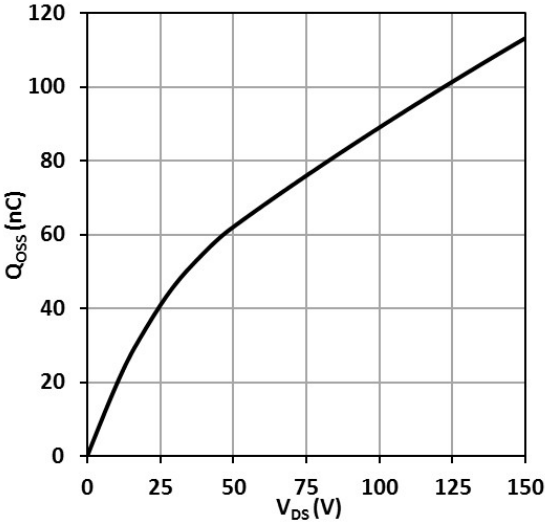


Fig. 15 Output Capacitance Stored Energy

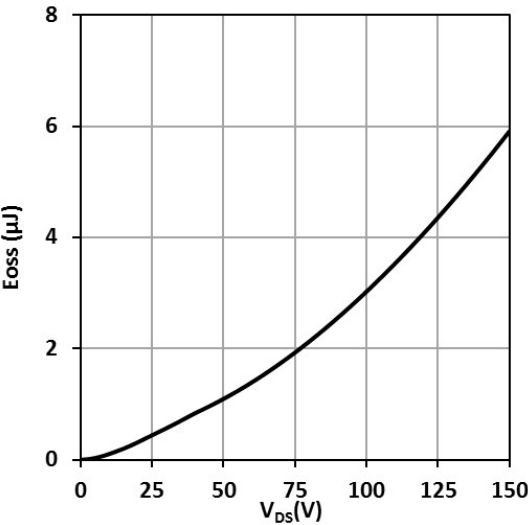


Fig. 16 Power Dissipation

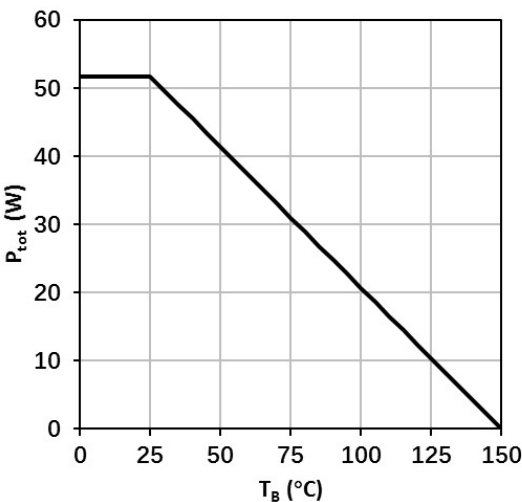


Fig. 17 Safe Operating Area

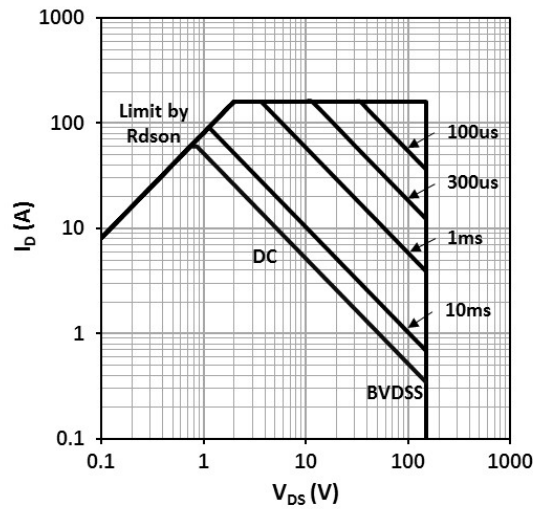
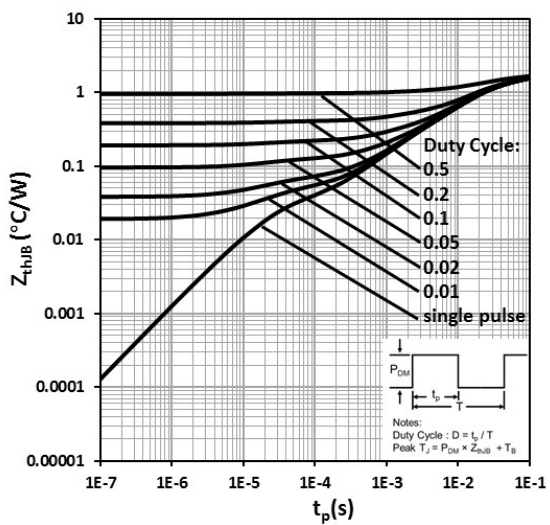
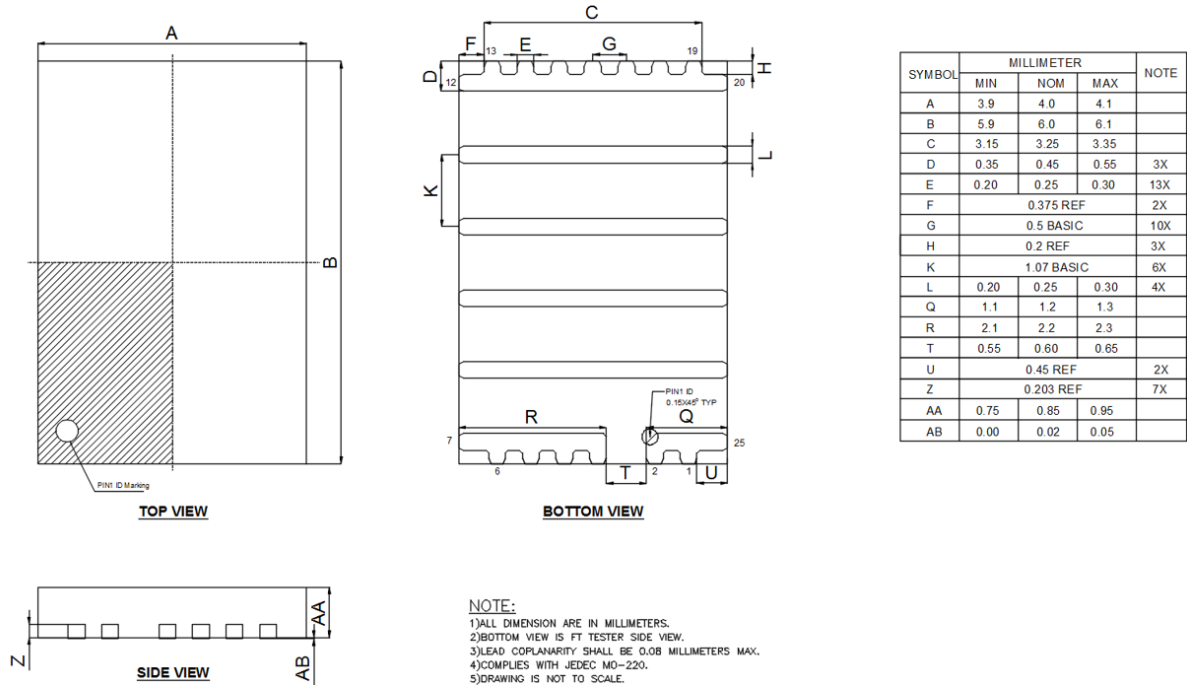


Fig. 18 Max. Transient Thermal Impedance

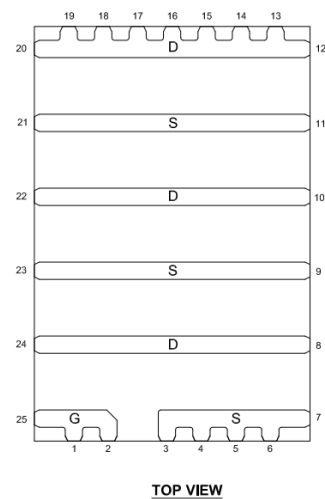


10. Package outlines

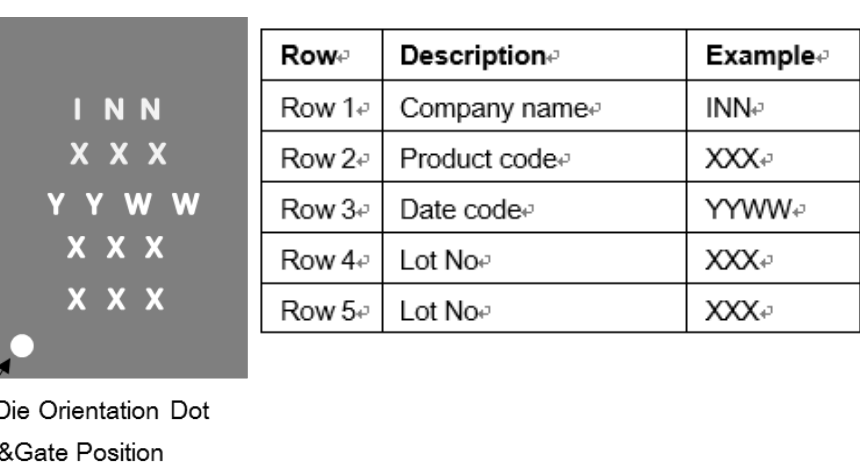
Package Reference



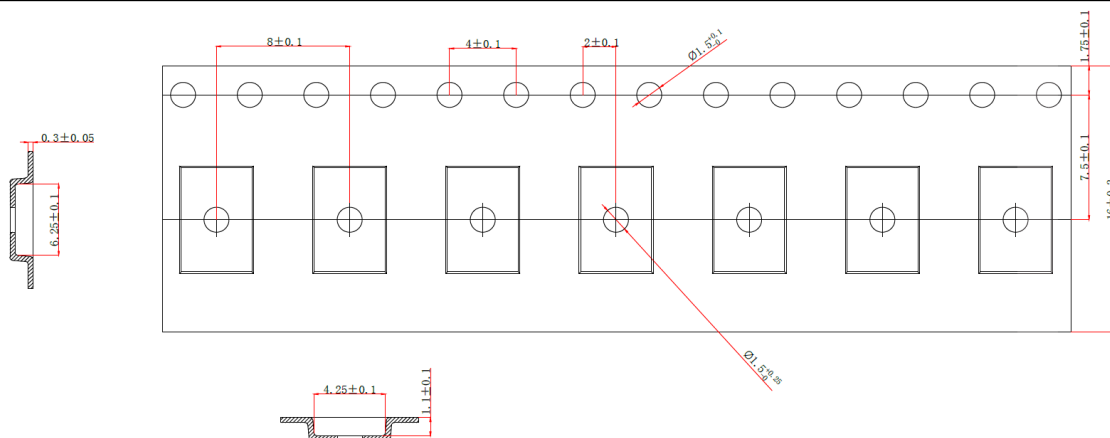
PIN configuration



Marking Reference

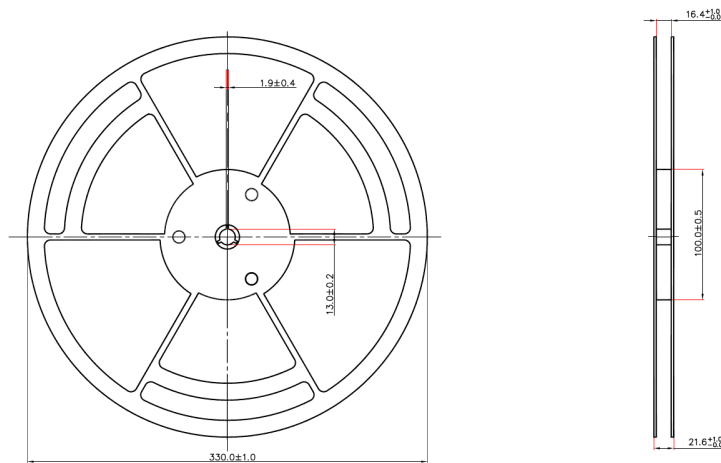


11. Reel information



NOTES:

1. CARRIER TAPE COLOR: BLACK.
2. COVER TAPE WIDTH: 13.3±0.10.
3. COVER TAPE COLOR: TRANSPARENT.
4. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20 MAX.
5. CAMBER NOT TO EXCEED 1MM IN 100MM.
6. MOLD# QFN/DFN/MIS6X4X0.75/0.85.
7. ALL DIMS IN MM.
8. BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING.

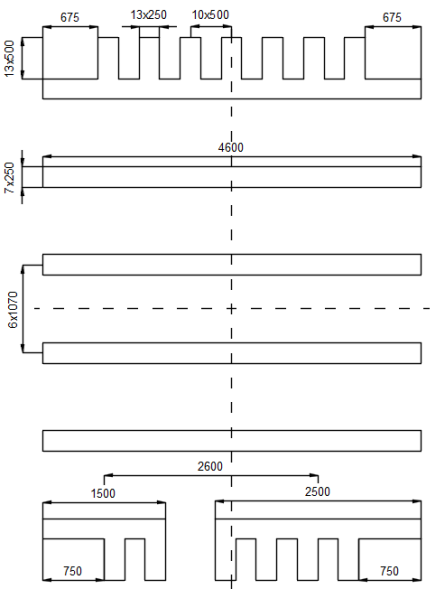


NOTES:

1. 2500 UNITS PER TRAY.
2. COLOR: WHITE.
3. ALL DIM IN mm.
4. GENERAL TOLERANCE±0.25.
5. BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING.
6. THE DERECTION OF VIEW:

12. Land Pattern

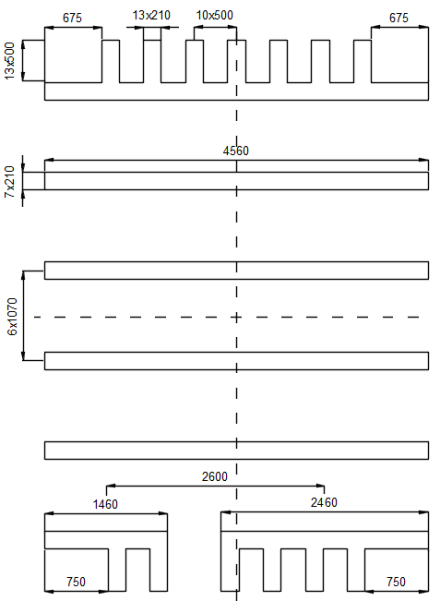
Recommended land pattern



TOP VIEW

Unit: μm

Recommended Stencil drawing



TOP VIEW

Unit: μm

13.Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2023-11-29	Version 1.0 release
1.1	2024-03-04	Add $V_{DS(tr)}$ in Table 4.

Important Notice

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